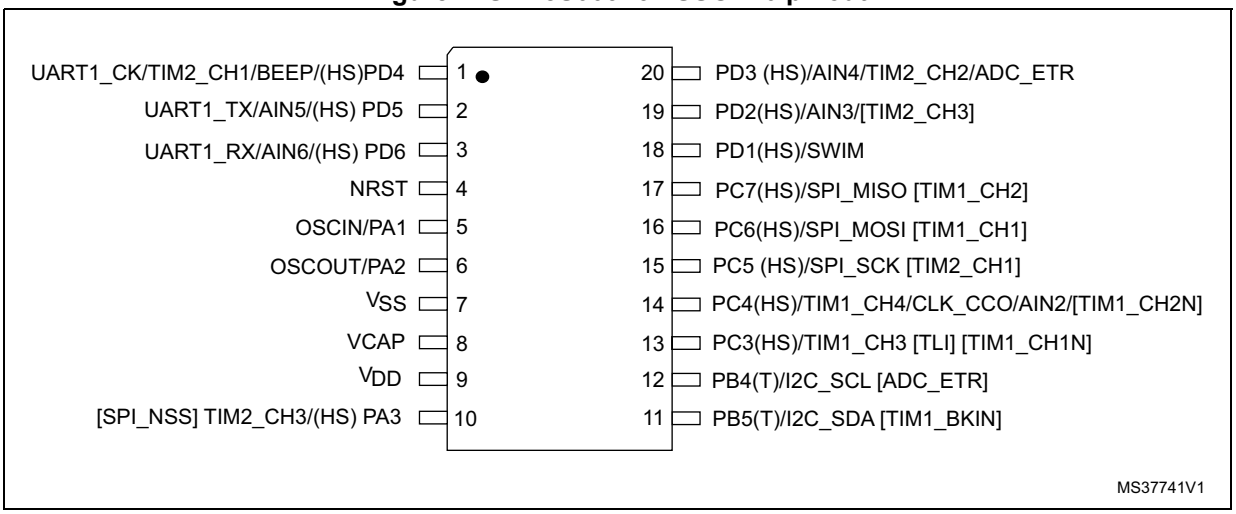
5.2 STM8S003F3 TSSOP20/UFQFPN20 pinout and pin description

Figure 4. STM8S003F3 TSSOP20 pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8S003F3 pin description

Pin no.		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
TSSOP20	UFQFPN20			floating	wpu	Ext. interr.	High sink(1)	Speed	OD	PP			
1	18	PD4/ BEEP/ TIM2_ CH1/ UART1 _CK	I/O	X	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output/ UART1 clock	-
2	19	PD5/ AIN5/ UART1 _TX	I/O	X	X	X	HS	O3	X	X	Port D5	Analog input 5/ UART1 data transmit	-
3	20	PD6/ AIN6/ UART1 _RX	I/O	X	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
4	1	NRST	I/O	-	X	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN(2)	I/O	X	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	X	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM2_ CH3 [SPI_ NSS]	I/O	X	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
11	8	PB5/ I2C_ SDA [TIM1_ BKIN]	I/O	X	-	X	-	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_ SCL	I/O	X	-	X	-	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3 [TLI] [TIM1_ CH1N]	I/O	X	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 - inverted channel 1 [AFR7]

Table 6. STM8S003F3 pin description (continued)

Pin no.		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
TSSOP20	UFQFPN20			floating	wpu	Ext. interr.	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/ [TIM1_ CH2N]	I/O	X	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	X	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	X	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	X	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM(4)	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/ [TIM2_ CH3]	I/O	X	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	X	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended d to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 12: Option bytes* below. Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 12. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC[7:0]								0x00
0x4802		NOPT1	NUBC[7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805	Misc. option	OPT3	Reserved			HSITRIM	LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	0x00
0x4806		NOPT3	Reserved			NHSITRIM	NLSI_EN	NIWDG_HW	NWWDG_HW	NWWDG_HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	0x00
0x4808		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT[7:0]								0x00
0x480A		NOPT5	NHSECNT[7:0]								0xFF

Table 13. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*

Table 13. Option byte description (continued)

Option byte no.	Description
OPT1	**UBC[7:0]** *User boot code area* 0x00: no UBC, no write-protection 0x01: Pages 0 defined as UBC, memory write-protected 0x02: Pages 0 to 1 defined as UBC, memory write-protected Page 0 and page 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory-write protected. *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM**: high-speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wakeup unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilization time. 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

Table 15. STM8S003F3 alternate function remapping bits for 20-pin devices

Option byte number	Description
OPT2	**AFR7***Alternate function remapping option 7* 0: AFR7 remapping option inactive: default alternate function(1) 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N. **AFR6** *Alternate function remapping option 6* Reserved. **AFR5** *Alternate function remapping option 5* Reserved. **AFR4** *Alternate function remapping option 4* 0: AFR4 remapping option inactive: default alternate function(1). 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. **AFR3** *Alternate function remapping option 3* 0: AFR3 remapping option inactive: default alternate function(1) 1: Port C3 alternate function = TLI. **AFR2** *Alternate function remapping option 2* Reserved. **AFR1** *Alternate function remapping option 1* (2) 0: AFR1 remapping option inactive: default alternate function(1) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3. **AFR0** *Alternate function remapping option 0(2)* 0: AFR0 remapping option inactive: Default alternate functions(1) 1: Port C5 alternate function = TIM2_CH1; port C6 alternate function = TIM1_CH1; port C7 alternate function = TIM1_CH2.

1. Refer to the pinout description.
2. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.